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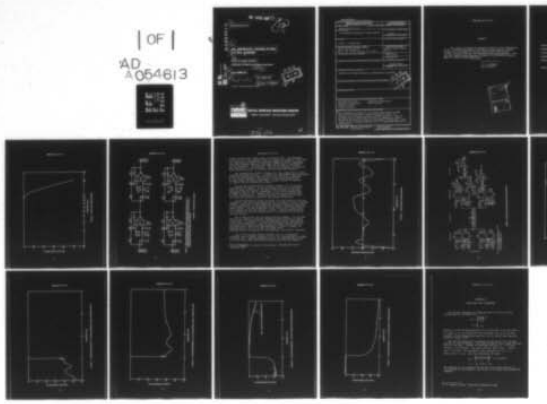

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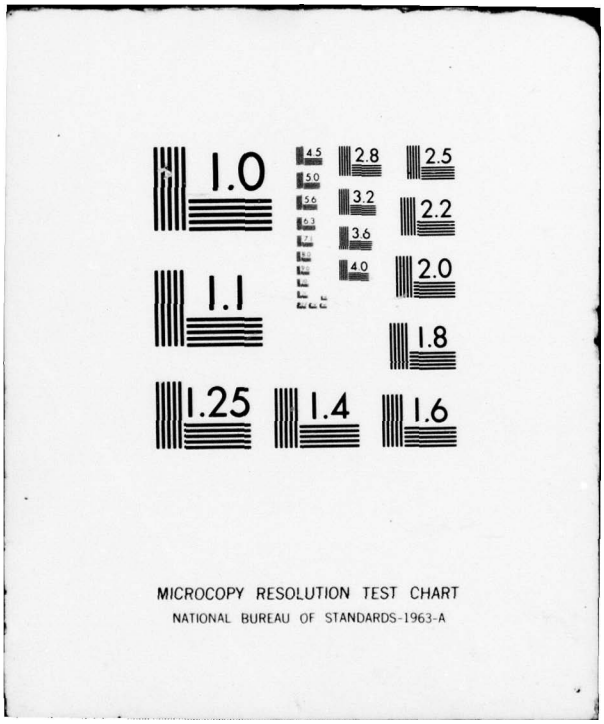
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(10) BY ARTHUR D. DELAGRANGE

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The translating filter is a new device developed at NSWC which gives an extremely steep attenuation slope at a variable but extremely accurate cutoff frequency. This is accomplished by using fixed filters and moving the signal frequency spectrum by frequency translation techniques. This report gives a complete description of an improved version of the device.

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SUMMARY

This report describes an improved version of the translating filter, a device developed at the Naval Surface Weapons Center. It will be of interest to persons working with sharp-cutoff filters, variable filters, or frequency-translation systems. Work was done under several projects, primarily the BEARTRAP program, Task No. A5335330/004D/8W04900000.

J. A. FAULKNER
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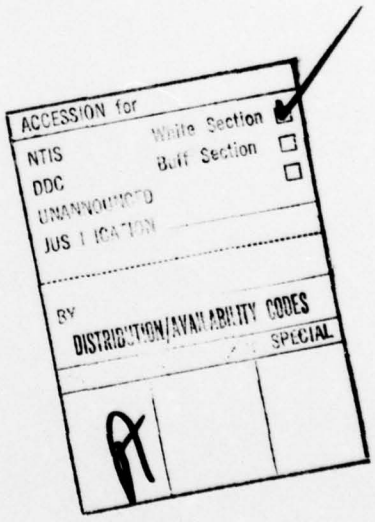


CONTENTS

ILLUSTRATIONS

TABLES

AN IMPROVED TRANSLATING FILTER DESIGN

INTRODUCTION

Reference (1) describes the translating filter, a new approach to variable-frequency high-pass/low-pass filter design which gives cutoff accuracy and steepness not attainable with conventional variable filters. The device was an outgrowth of other systems designed for use in Code CU22. All circuitry in the first model was borrowed from other existing systems and was modified to suit the purpose; none was developed specifically for the translating filter. Consequently, performance was considerably less than desired. However, the device not only worked well enough to prove the concept but well enough to find considerable use in the branch. Advances in circuit design made on other projects promised improvement in virtually all sections of the translating filter. These advancements were incorporated into a second unit. This report describes the new unit completely. (Reference (1) left out some details for the sake of brevity.)

The translating filter obtains a very steep cutoff slope by shifting the frequency spectrum of the input signal to a more convenient location in the spectrum where a fixed filter is used. This technique has been used for some time for narrowband filtering. To extend the technique to broadband, SSB (Single-Sideband) techniques must be used; this necessitated the development of practical broadband phase shifters.

The frequency translation is controlled by a frequency synthesizer, giving extremely accurate frequency control. The steepness of the slope is determined by the minimum frequency the phase shifter can handle, not the number of filter poles or zeroes available. Passband flatness is not directly affected by filter poles or zeroes either. On the other hand, the maximum rejection is limited by the accuracy of the phase shifters. Total phase shift, and hence delay and transient response are

[1] A. D. Delagrange, "It Could be the Ideal Filter," ELECTRONIC DESIGN Magazine, Vol. 24, No. 4, 16 Feb 1976. (pp. 156-161).

are virtually uncontrolled in this type of filter. To summarize, in a conventional variable-frequency filter the critical design problem is the number and accuracy of variable filter pole and zero frequencies, while in a translating filter the critical design problem is the accuracy of fixed broadband phase-shifters. Each method has advantages and disadvantages; the properties of the translating filter relative to a conventional filter are summarized in Table (1).

OPERATION

Figure (1) shows a block diagram of the translating filter; Figure (2) shows the (double-sided) frequency spectrum of the signal at various points in the system when used in the low-pass mode. As with all sampled or carrier systems, the input must be band-limited to avoid spectrum-foldover, also known as "aliasing". This is done by a fixed linear low-pass prefilter having a cutoff frequency of 14 kHz.

The signal then passes through a phase-shift network, where the amplitude is unchanged but the phase difference between the two ouputs is 90°. These two outputs are modulated up in frequency by quadrature phases of a fixed carrier frequency (100 kHz) and summed. Balanced-modulators are used instead of linear multipliers, so the harmonics are removed by a fixed 150 kHz low-pass filter. The spectrum at point "A" (see Figure (2)) has been shifted up by 100 kHz and the lower sideband has been eliminated. Dotted lines indicate portions of the spectrum removed by cancellation. This so far is conventional SSB modulation.

The signal is then modulated down by quadrature phases of a variable frequency (100 kHz + Δf), phase-shifted 90° and summed. The frequency difference Δf will turn out to be the system cutoff frequency. A fixed 23 kHz low-pass filter removes the double-frequency components and harmonics. The signal spectrum at point "B" (see Figure (2)) has now been shifted partly through zero, and that part of the spectrum not shifted through zero has been eliminated by cancellation. This is sort of SSB-in-reverse. The filtering has actually been performed by comparing the input spectrum to a reference frequency by differencing. What remains is to return the remaining portion of the signal to its original location in the frequency spectrum.

The signal next goes to a 3.6 Hz high-pass filter. The phase shifters do not work properly below this frequency, so these frequency components must be removed, or they will show up in the output as extraneous signals near the cutoff frequency.

The signal once again goes through a phase shifter, is modulated up by quadrature phases of the variable frequency, summed and low-pass filtered. The signal spectrum at point "C" (see Figure (2)) is the desired part of the input spectrum but shifted up by 100 kHz. Here the upper sideband is eliminated.

TABLE 1.

PROPERTIES OF TRANSLATING FILTER

ADVANTAGES	DISADVANTAGES
1. Cutoff frequency is set digitally.	1. Component count is large.
2. Cutoff frequency is settable to within 1 Hz.	2. Stopband attenuation is about 40 dB maximum.
3. Attenuation is 40 dB at the cutoff frequency.	3. System is nonlinear; extraneous frequencies are generated.
4. Passband is essentially flat to within 10 Hz of cutoff.	4. Phase shift is large and nonlinear; transient response is poor.
5. No high-accuracy components need be variable.	5. Low-pass mode does not include DC.
6. Cutoff frequency may be programmed externally.	6. Passband gain is not inherently unity.
	7. Changing cutoff frequency setting requires delay while system settles.

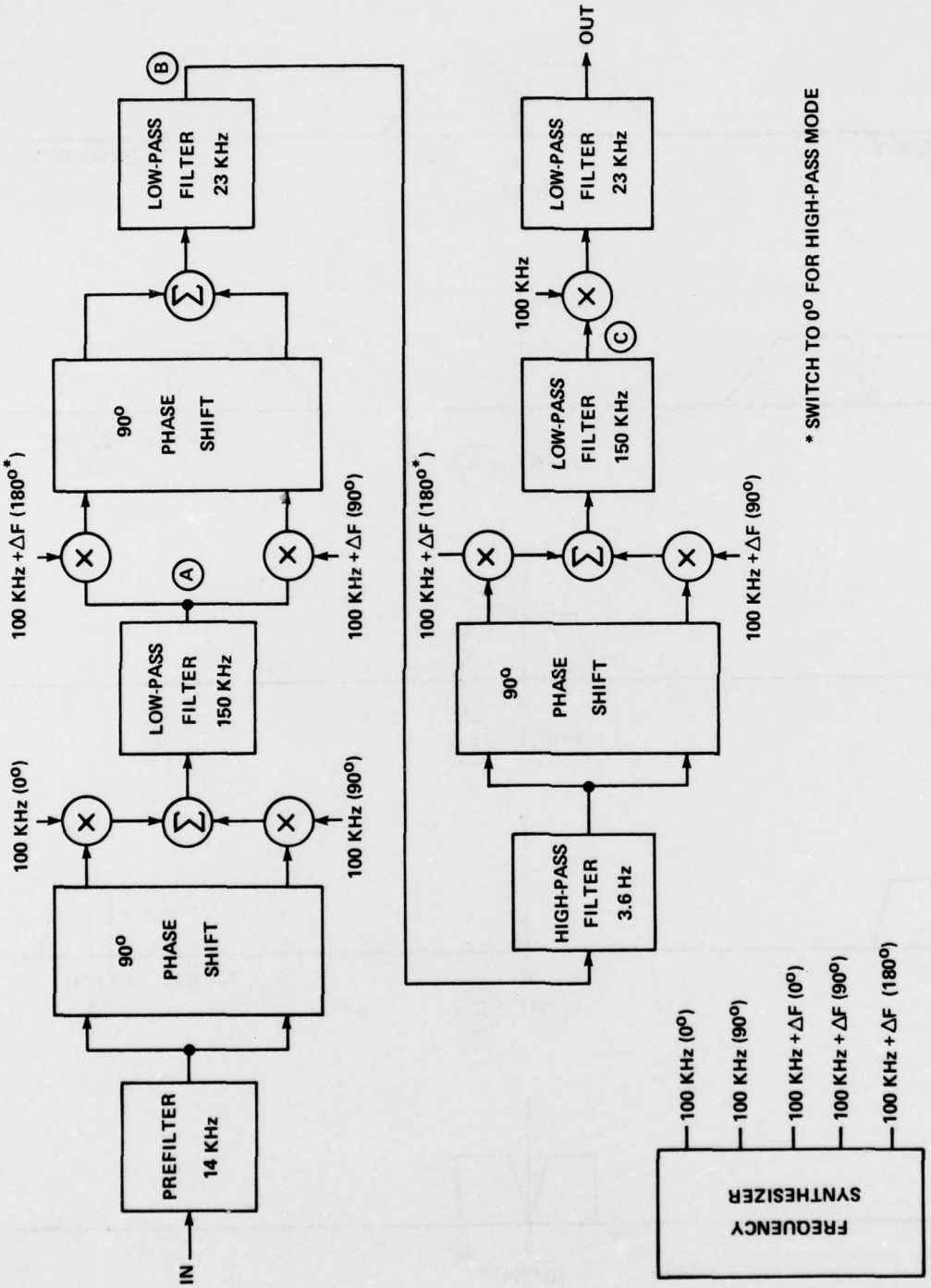


FIGURE 1. FILTER SYSTEM BLOCK DIAGRAM

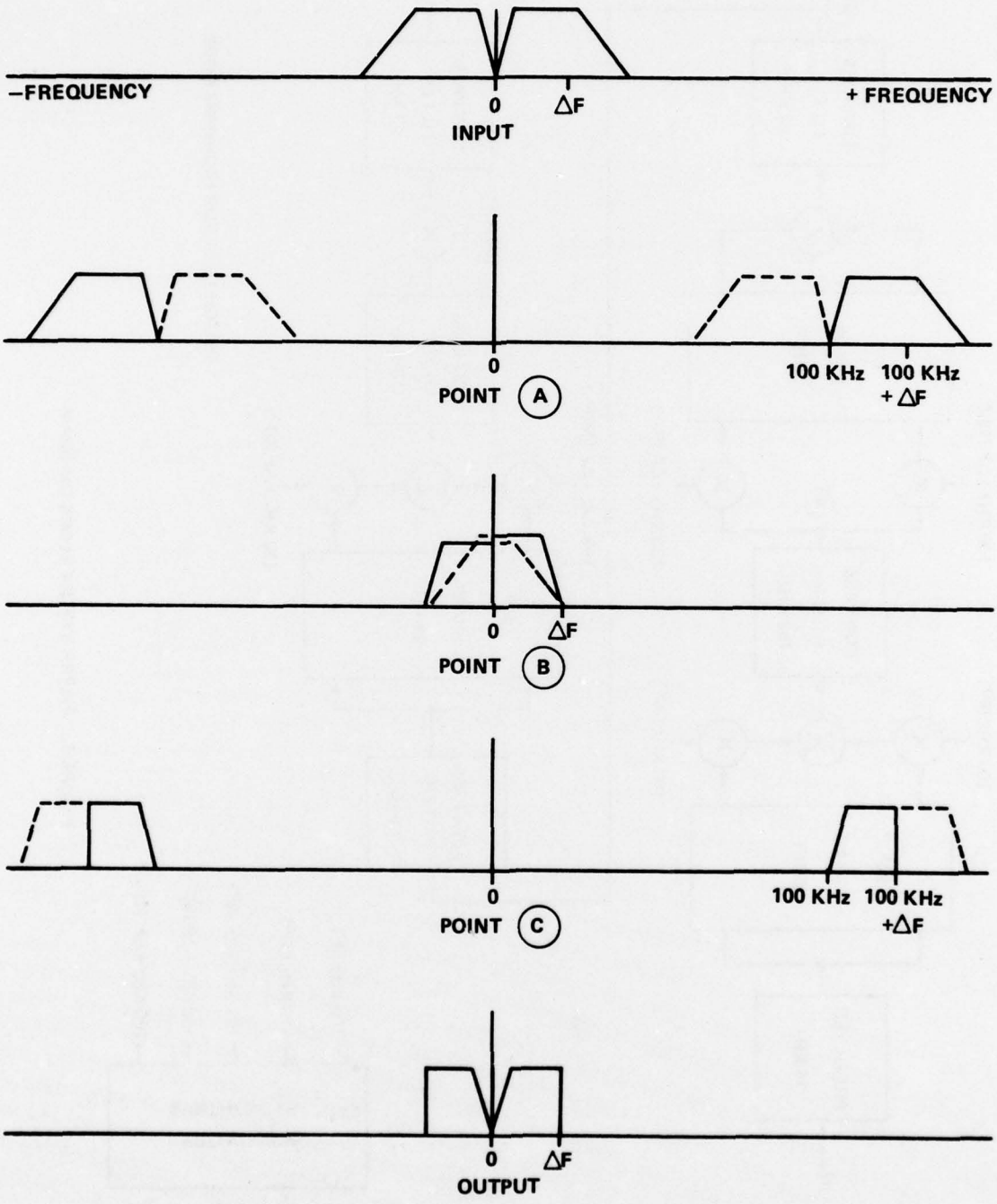


FIGURE 2. SYSTEM FREQUENCY SPECTRA, LOW-PASS MODE

To obtain the final output, this signal is down-modulated by an arbitrary phase of the 100 kHz and low-pass filtered (23 kHz again.) SSB modulation is not necessary here, as only one sideband is present.

To make the overall filter function in a high-pass instead of low-pass mode, all that is necessary is to invert the driving signal in one of each pair of variable-frequency (100 kHz + Δf) modulators. This causes the parts of the spectrum at points "B" and "C" that previously cancelled to now add instead, and vice-versa. The frequencies and phases necessary for the modulators are supplied by an internal frequency synthesizer.

CIRCUITRY

The prefilter (Figure (3)) is a seven-pole, low-pass unity-gain active ladder filter (reference (2)). The frequency response is shown in Figure (4). All filters will be referred to by the calculated cutoff frequencies; actual values will differ somewhat because the calculations are approximate (reference (2)). The cutoff frequency is chosen according to the following requirements: Response must be flat to 10 KHz, the signal band of the system. Attenuation must be adequate at 100 kHz, the carrier frequency used. It is also desirable that the prefilter reject as much as possible above 10 kHz, as this is the upper limit of the phase shifters; frequencies above this will be handled improperly by the system. In particular, in the low-pass mode frequencies above 10 kHz will not be rejected no matter what the cutoff setting.

The phase shifter circuit (Figure (5)) is the critical part of the system. No finite circuit can generate exactly 90° phase shift over a finite frequency range without attenuation so the circuit must give an approximation to constant phase shift. The circuit (reference (3)) consists of a chain of pairs of all-pass networks that have a gain of unity but a phase lag that increases from 0° at low frequency to 180° at high frequency. Each pair gives a phase difference that peaks near 90° between the break-point frequencies. These are spaced approximately logarithmically so that the overall phase difference stays near 90° with a constant "ripple"

[2]Arthur D. Delagrange, "A Useful Filter Family," NSWC/WOL TR 75-150, October, 1975.

[3]J. Graeme, "Applications of Operational Amplifiers; Third-Generation Techniques Mc-Graw Hill, 1973.

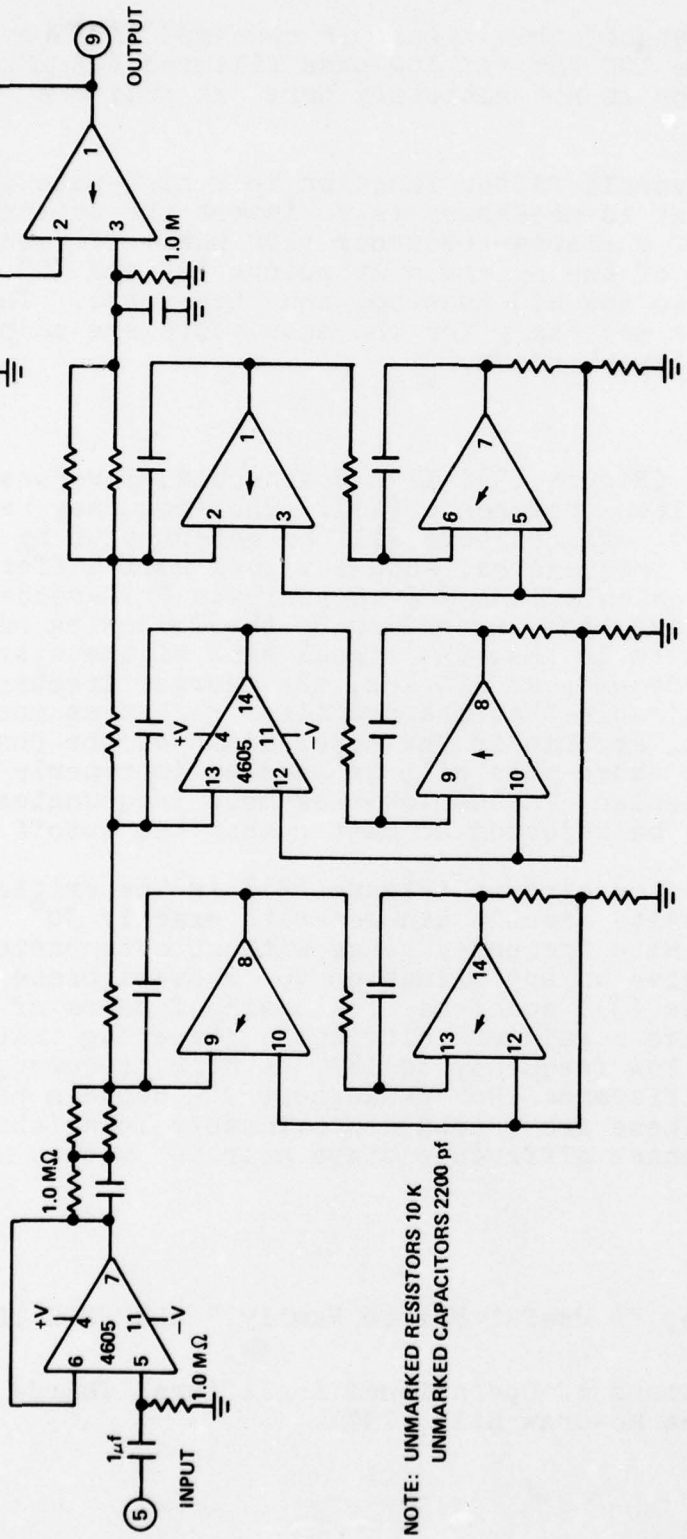


FIGURE 3. 14 KHz LOW-PASS PREFILTER CIRCUIT

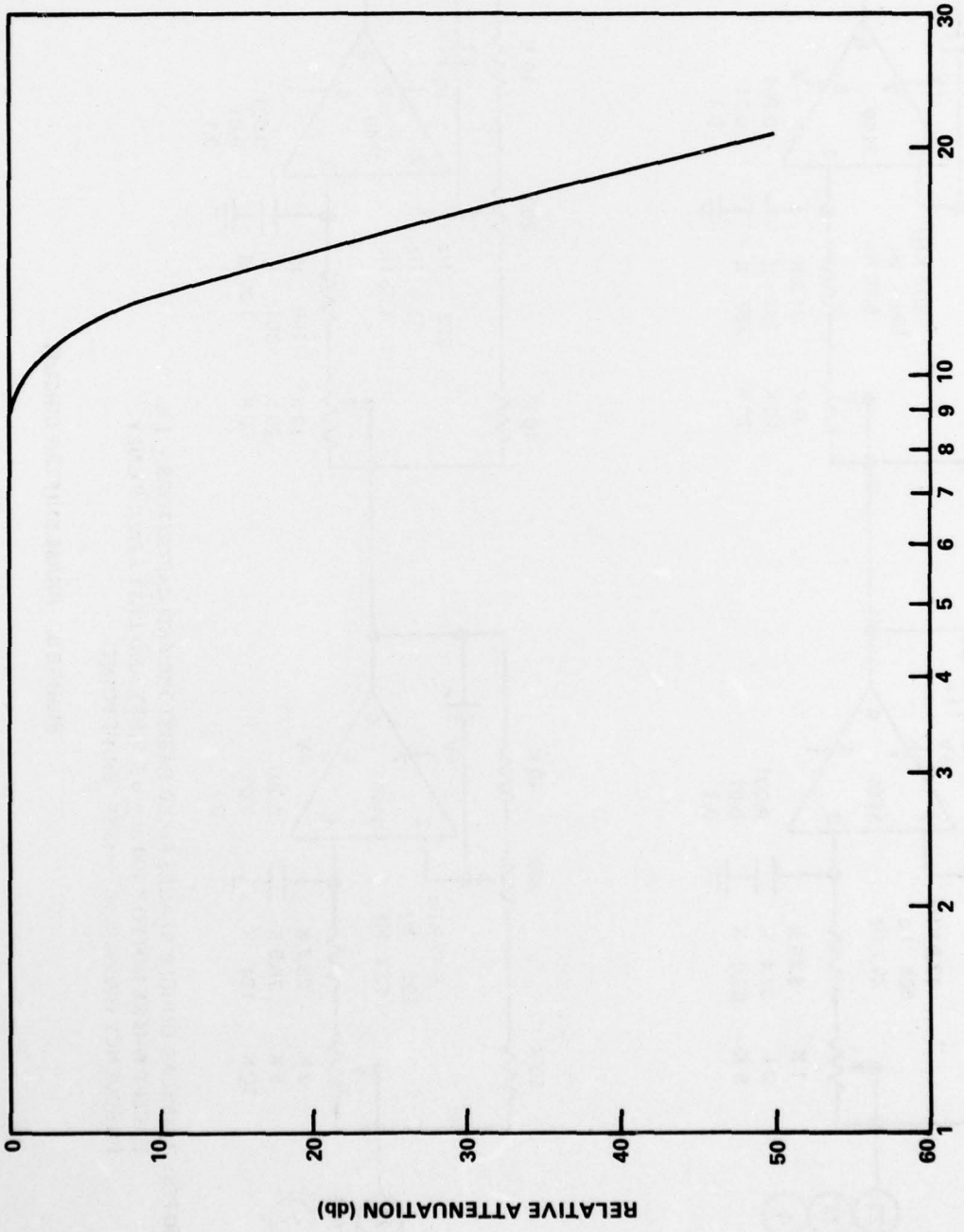
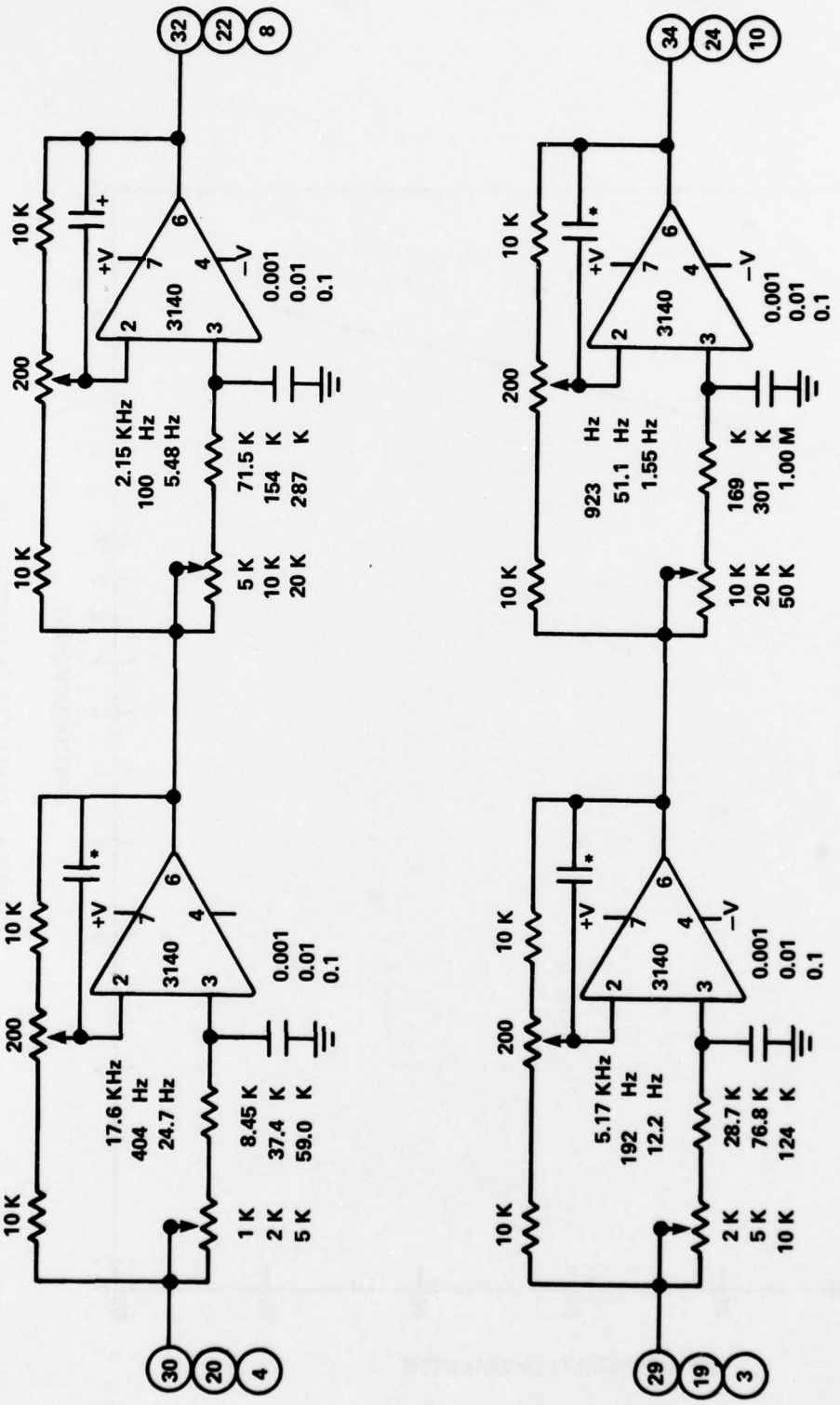


FIGURE 4. PREFILTER CHARACTERISTIC



NOTES: 3 SIMILAR DOUBLE STAGES FIXED RESISTORS AND CAPACITORS ± 1 %
EXCEPT WHERE NOTED * 100 pf ± 5 % FIRST AND LAST STAGES ONLY
FREQUENCY GIVEN IS 90° PHASE SHIFT POINT

FIGURE 5. PHASE SHIFTER CIRCUIT

above and below the correct value (see Figure (6)). The magnitude of this error is the limiting factor on system performance. Note that the ripple may be reduced by using more stages at closer intervals; also that frequency range of the phase shifter limits the bandwidth of the instrument. The practical limit on accuracy of resistors and capacitors is ± 1% tolerance. This is not adequate, so potentiometer adjustments must be included for both gain and frequency.

The up-modulators (refer to Figure (7)) are conventional double-balanced modulator circuits. A carrier-null adjustment must be provided, as carrier leakthrough would show up in the output as a component at the cutoff frequency. The outputs of the two modulators may be added simply by paralleling them; a balance adjust is required to correct for the difference in gains.

The 150 kHz low-pass filter (refer to Figure (7)) is a seven-pole passive LC ladder. The output resistors of the up modulators form the input termination; the input bias resistors of the down modulators form the output termination. The filter characteristic is shown in Figure (8). Response must be flat in the signal band, ± 10 kHz around 100 kHz. Attenuation must be adequate at 300 kHz, the first odd harmonic produced by the balanced modulators.

The down-modulators (refer to Figure (7)) are similar to the up-modulators. The first down-modulators are followed by a pair of op-amp buffers. Simple RC low-pass/high-pass sections reduce the slew rate to the capabilities of the op-amps and provide AC coupling before the phase shifter. The down-modulator in the second half of the system is a single, and does not require a buffer. Carrier feedthrough is not a problem in the down modulators as it is removed by the 23 kHz low-pass filters.

The 23 kHz filters are three-pole passive ladders. In the first half of the system the resistor summing network provides the input termination. In the second half the modulator output load resistor is the input termination. In both cases resistors are provided for the output termination; op-amps buffer the output and provide the necessary gain. The filter characteristic is shown in Figure (9). Response must be flat to 10 kHz, the signal band. Attenuation must be adequate at 200 kHz, twice the carrier frequency.

The 3.6 Hz high-pass filter (Figure (10)) is a seven-pole unity-gain active ladder (Reference (2)). The characteristic is shown in Figure (11). Response should be as flat as possible down to near 3 Hz, the lower limit of the phase shifter, and then drop steeply.

[2] A. D. Delagrange, "A Useful Filter Family," NSWC/WOL TR 75-150, October, 1975.

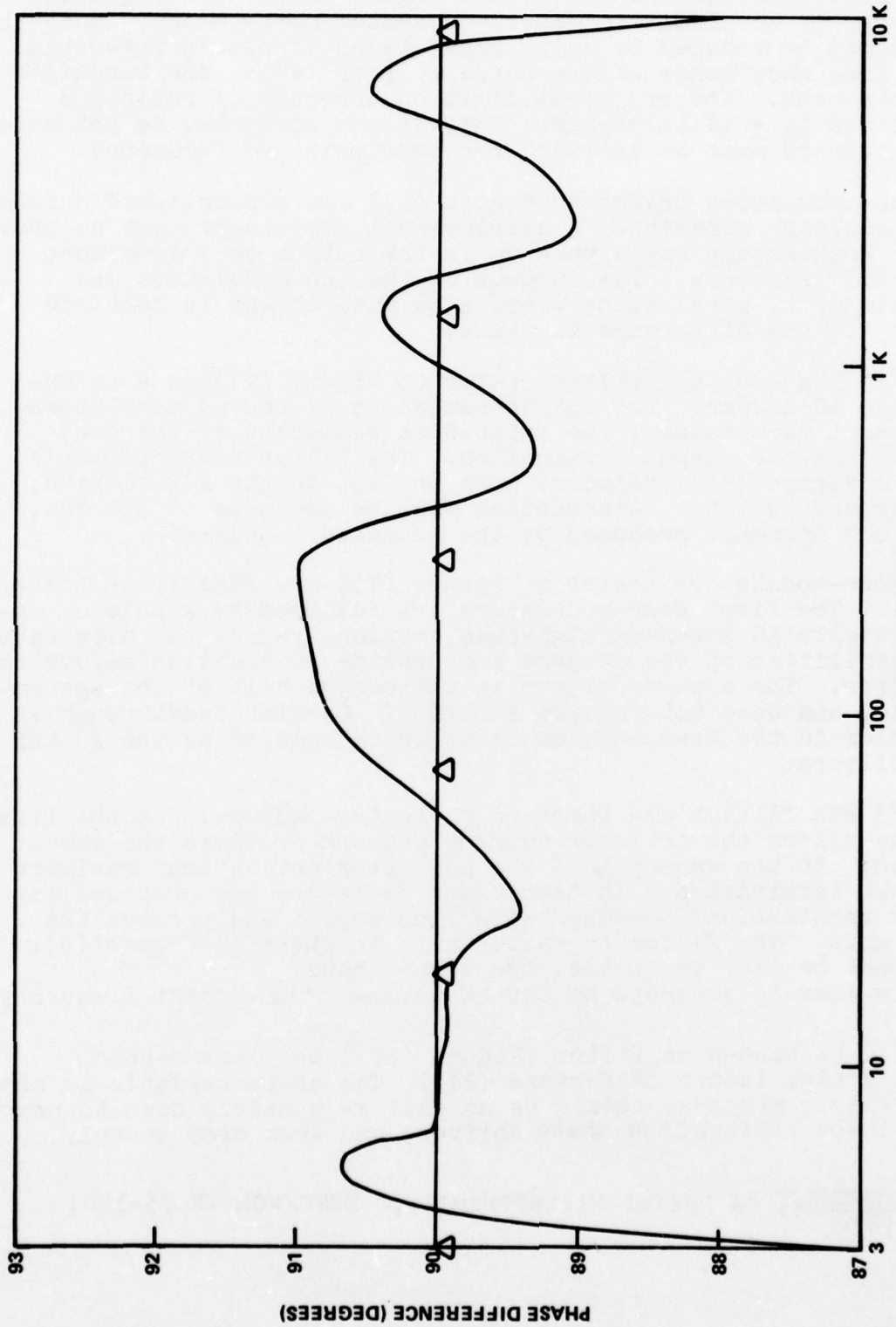


FIGURE 6. PHASE-SHIFTER CHARACTERISTIC

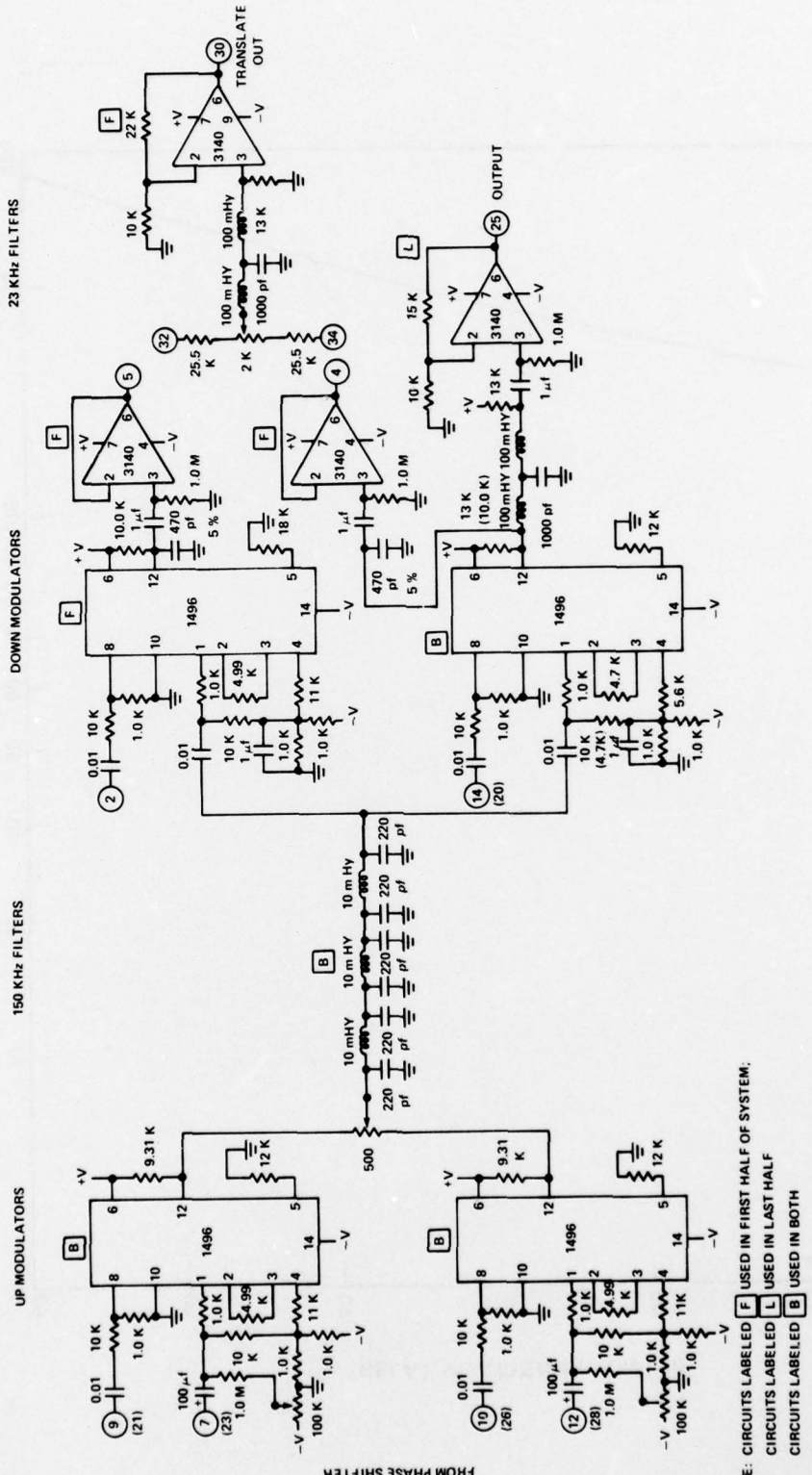


FIGURE 7. MODULATOR AND LOW-PASS FILTER CIRCUITS

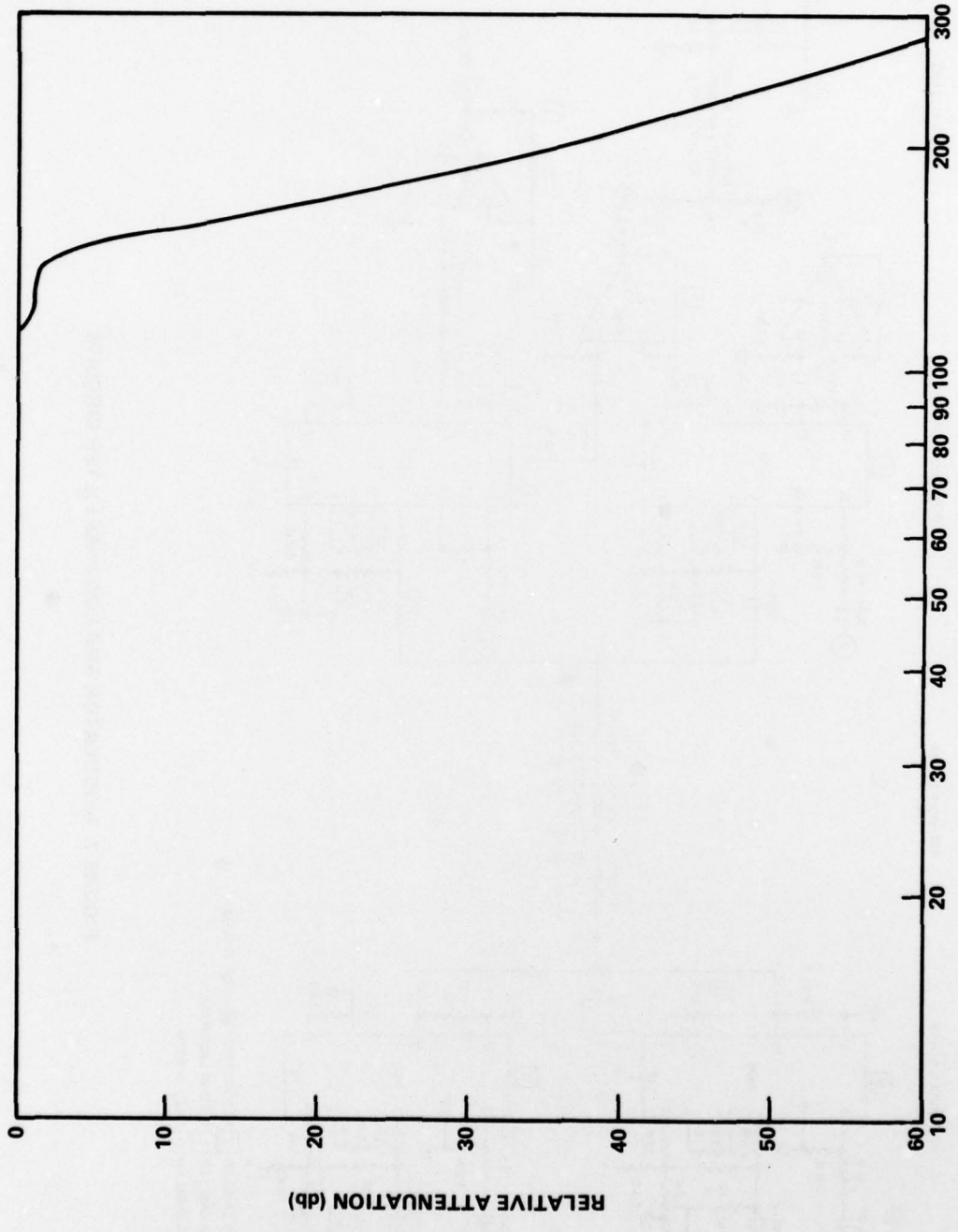


FIGURE 8. 150 KHz LOW-PASS FILTER CHARACTERISTIC

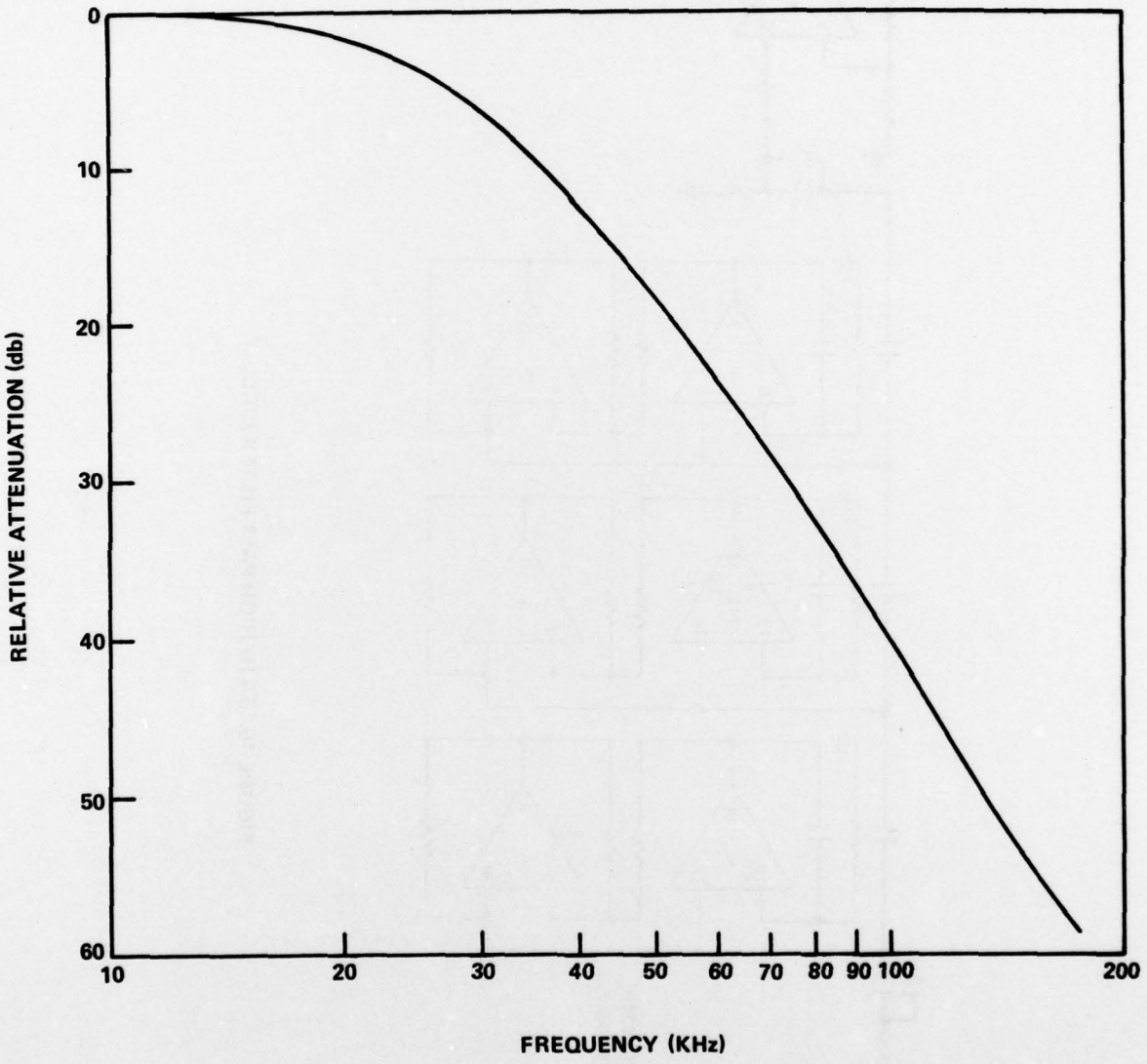


FIGURE 9. 23 KHz LOW-PASS FILTER CHARACTERISTIC

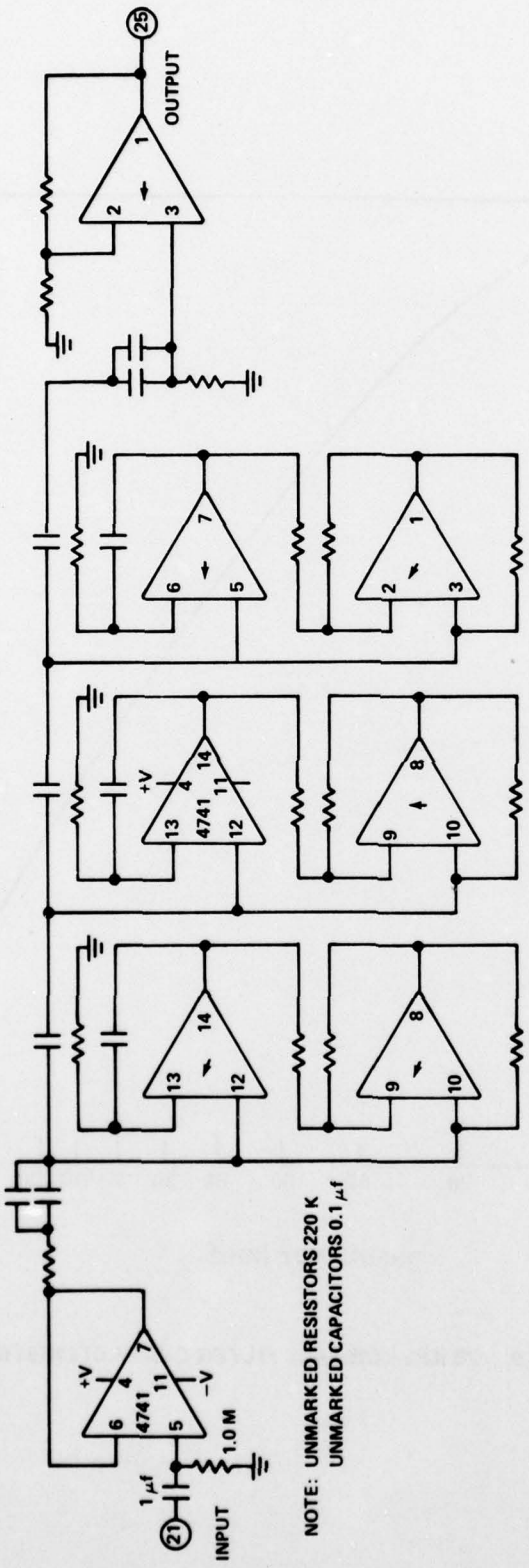


FIGURE 10. 3.6 Hz HIGH-PASS FILTER CIRCUIT

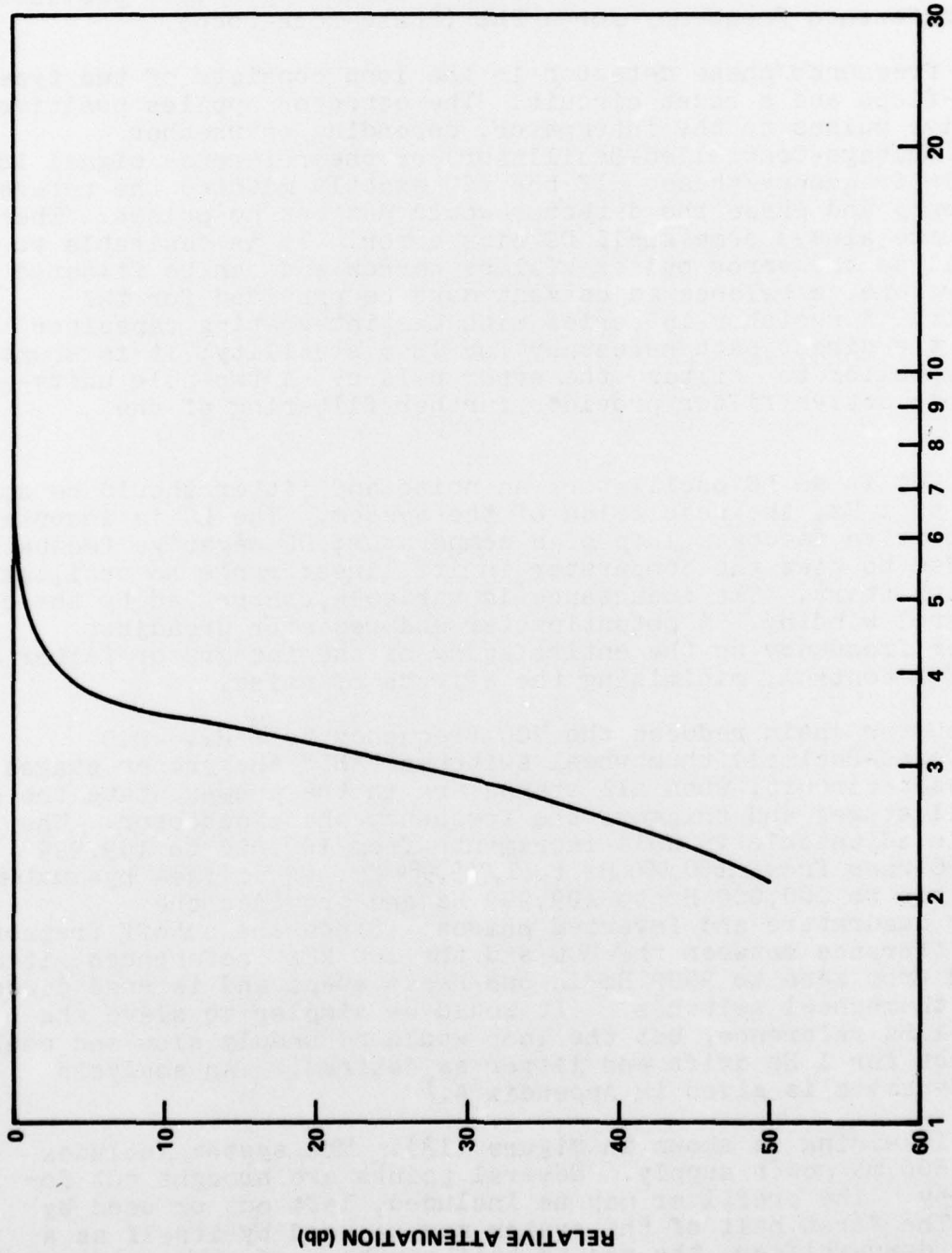


FIGURE 11. 3.6 Hz HIGH-PASS FILTER CHARACTERISTIC

The frequency synthesizer (Figure (12)), (reference (4)) is of simple design and uses CMOS (Complemntary-Metal-Cxide Semiconductor digital lcgic. A 400 kHz crystal oscillator is divided by four to provide the quadrature phases of the 100 kHz. A divide-by-25,000 provides a 16 Hz reference frequency for a PLL (Phase-Lock-Loop).

The frequency/phase detector in the loop consists of two type "D" flip-flops and a reset circuit. The detector applies positive or negative pulses to the integrator, depending on whether the VCO (Voltage-Controlled-Oscillator) or the reference signal is greater in frequency/phase. If the VCO exactly matched the reference in frequency and phase the detector would put out no pulses. There is of course always some small DC bias error. It is desirable to keep this small so the error pulses will be narrow and can be filtered out; therefore, a balance adjustment must be provided for the integrator. A resistor in series with the integrating capacitor provides the direct path necessary for loop stability; it is shunted with a capacitor to filter the error pulses. A two-pole unity-gain Butterworth active filter provides further filtering of the pulses.

The VCO is an LC oscillator, as noise and jitter should be small compared to 1 Hz, the resolution of the system. The LC is inserted in the positive feedback loop of a comparator; DC negative feedback is provided to bias the comparator in its linear range so oscillation will always start. The inductance is variable,controlled by the current in a control winding. A potentiometer and resistor preadjust the center frequency so the entire swing of the integrator/filter may be used for control, minimizing the effects of noise.

A counter chain reduces the VCO frequency to 16 Hz. BCD (Binary Coded-Decimal) thumbwheel switches "AND" the proper stages into a reset circuit; when all stages are in the proper state the gate resets all stages and triggers the frequency/phase detector. The divider is adjustable in unit increments from 100,000 to 109,999 so the VCO runs from 1,600,000 Hz to 1,759,984 Hz. A divide- by- sixteen reduces this to 100,000 Hz to 109,999 Hz and provides the necessary quadrature and inverted phases. Since the cutoff frequency is the difference between the VCO and the 100 kHz references, it may be varied from zero to 9999 Hz in one-Hertz steps and is read directly from the thumbwheel switches. (It would be simpler to slave the PLL to a 1 Hz reference, but the loop would be unduly slow and could not correct for 1 Hz drift and jitter as desired. An analysis of loop dynamics is given in Appendix A.)

Chasis wiring is shown in Figure (13). The system includes a $\pm$ 15V, 500 ma power supply. Several points are brought out for flexibility. The prefilter may be included, left out or used by itself. The first half of the system may be used by itself as a frequency down-shifter, the second half may be used by itself as an up-shifter.

[4] V. Manassewitsch, Wiley, "Frequency Synthesizers; Theory and Design, 1976."

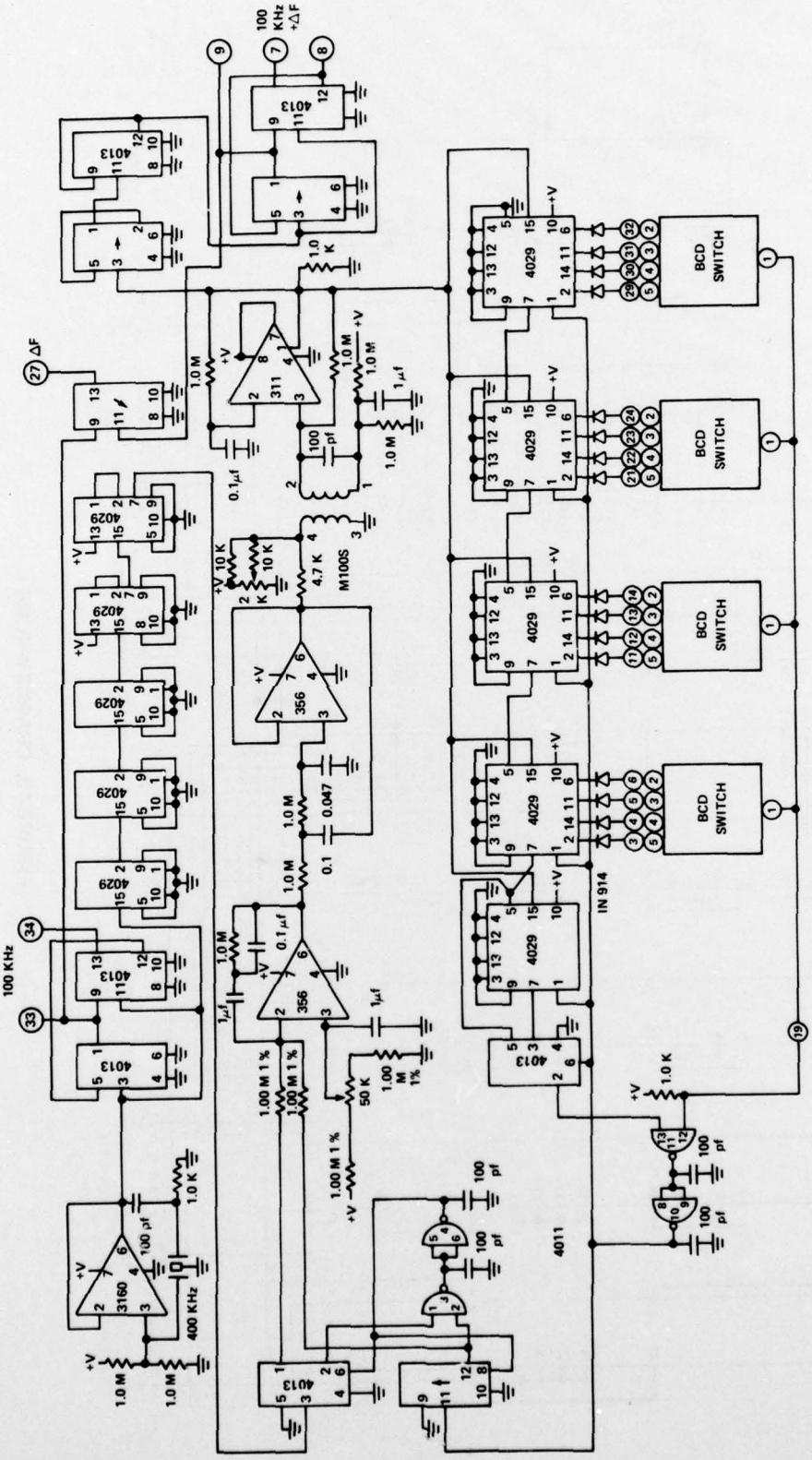


FIGURE 12. FREQUENCY SYNTHESIZER CIRCUIT

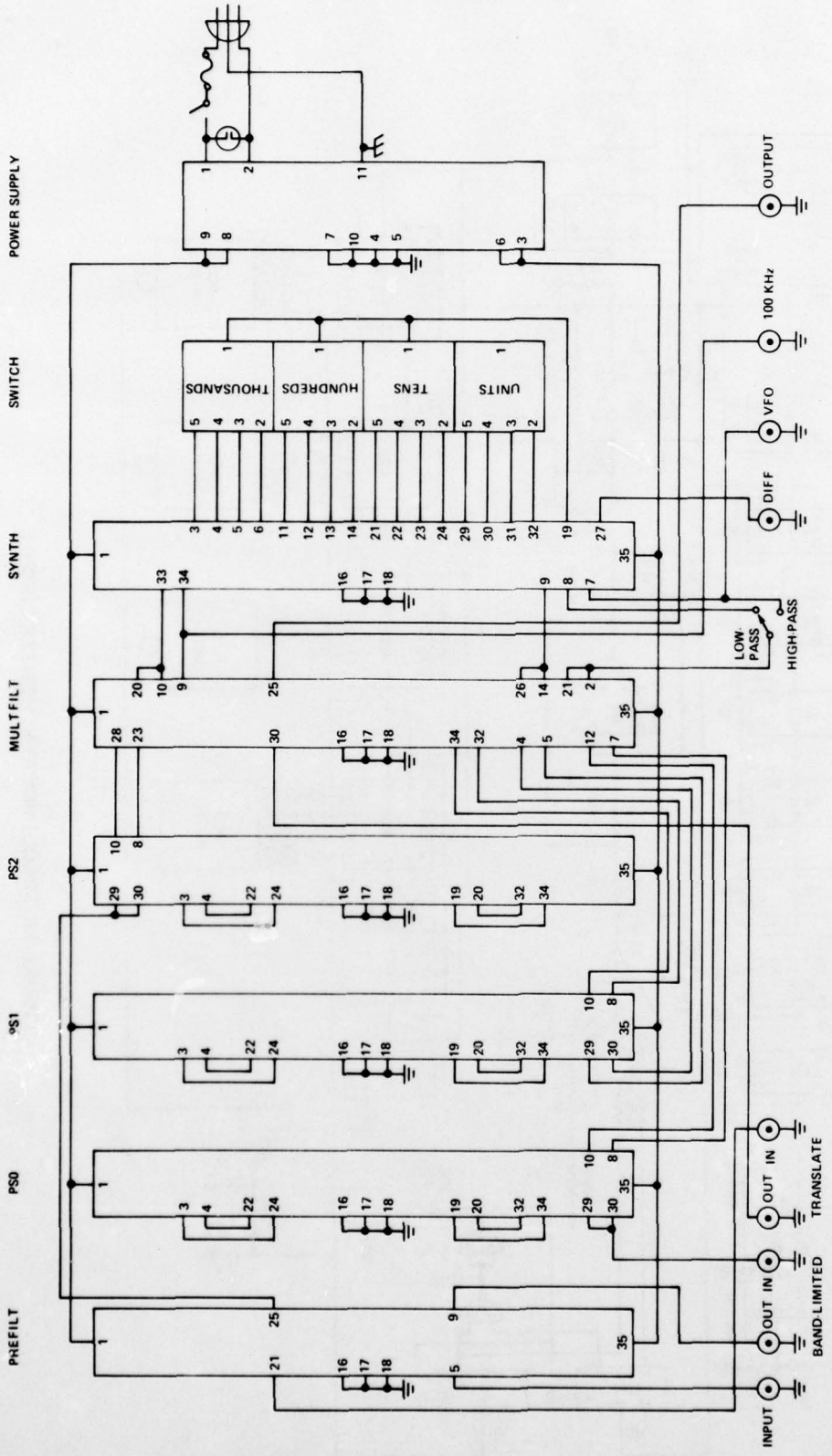


FIGURE 13. CHASSIS WIRING

ADJUSTMENT PROCEDURE

Each phase shifter is adjusted by itself as follows: Gain adjustments are made first, one stage at a time. Short the phase-shifting capacitor to ground so phase shift is 180°. Connect a pair of precisely matched resisors (1 kΩ) in series between the input and output of the stage. With a signal on the input (100 Hz 1 VRMS sine wave) adjust for a null at the junction of the matched resistors. Phase may now be adjusted, again one stage at a time. Referring to Figure (5) insert a sine wave (1 VRMS) at the frequency listed. Using a phasemeter connected to the input and output of the stage, adjust for 90° phase shift. The overall characteristic of the phase shifter is then checked. If the peaks and valleys do not stay within the allowable ± 1%, (refer to Figure (6)) the stage nearest the offending peak/valley is twiddled to bring it into conformance. (The triangles show the stage frequency locations.)

A conventional phasemeter was used for this procedure, but the low-frequency response was inadequate and the accuracy is marginal for this application. A better phasemeter could be built using the techniques of Reference (6) which would be highly accurate and immune to noise in the vicinity of 90°, all that is required here.

The frequency synthesizer is also adjusted by itself. Setting the thumbwheel switch on 5000, adjust the center frequency potentiometer so that the integrator/filter output is approximately half the supply voltage. To balance the integrator, set the thumbwheel switch on 0000, observe the VFO output on an oscilloscope triggered from the 100 kHz reference and adjust for minimum jitter. (The loop will have to resettle after each tweak.)

Next the carrier null adjustments may be set. With all the cards in the system, set the thumbwheel switch on 1000, short the BANDLIMITED input ground and adjust the first pair of balanced modulators alternately to achieve minimum 1000 Hz signal at the TRANSLATE output. Then short the TRANSLATE input and adjust the second pair for a minimum at the final output.

Finally the SSB cancellation adjustments may be made. With a 1000 Hz 1 VRMS sine wave in and the system set for 2000 Hz high-pass, adjust the balance at the input to the first 23 kHz filter to give minimum signal at the TRANSLATE output. Next change the thumbwheel switch setting to 0000 Hz low-pass and adjust the balance at the input to the first 150 kHz filter for minimum signal at the TRANSLATE output. Finally with a 1 VRMS sine wave as close as possible to 1000 Hz inserted in the TRANSLATE input and the system

[6] A. D. Delagrange, "Correlating Technique for Measurement of Phase, NOLTR 74-127, July, 1974.

set for 1000 Hz low-pass, adjust the balance at the input to the second 150 kHz filter for minimum 2000 Hz signal at the system output.

PERFORMANCE

High-pass and low-pass performances of the system are shown in Figures (14) and (15), respectively. These graphs were made by inserting a sine wave of variable frequency and measuring the total filter output with a true-RMS meter. Actual rejection of the input frequency is as good or better than this, because part of the output is at a different frequency. Performance with a broadband (noise) input is shown in Figures (16) and (17). These curves would be identical to Figures (14) and (15) for a linear filter, but the translating filter is not truly linear.

Leak-through from imperfect SSB cancellation due to a phase error θ is approximately $1/\theta$ (θ in radians), or about -36 dB for 1^{o} phase error. The in-phase components add almost perfectly, giving + 6 dB gain. However, the signal must pass through two critical SSB modulations in the low-pass mode, costing about 3 dB. As a rule of thumb then, $\pm$ 1^{o} phase accuracy gives a 40 dB system.

Rejection is about 10 dB better than the previous model (reference (1)). The new model actually does not work quite as close to the cutoff frequency as the old model. The old phase shifters used 1µf capacitors of poor quality to get down to 1 Hz; the new ones use precision capacitors where 0.1 µf is the maximum practical size, giving a lower limit of about 3.6 Hz. However, the new frequency synthesizer is settable in 1-Hz steps (the old was limited to 10-Hz steps), so this effect may be corrected manually by offsetting the cutoff frequency. Also, the old model had a $\pm$ 1 Hz band around cutoff where a strong signal would produce garbage in the output; this is prevented in the new model by the high-pass filter. Passband droop has been virtually eliminated in the new model. (The droop in Figure (16) is due to the measuring system, not the translating filter.) The new model works well to 10 kHz; the old one was useful only to about 5 kHz.

The system parameters (carrier frequency, phase shifter range) chosen for the new design are the best that could be achieved without a major redesign. They do not represent either the limits of the technique or what one would probably want in a general-purpose device.

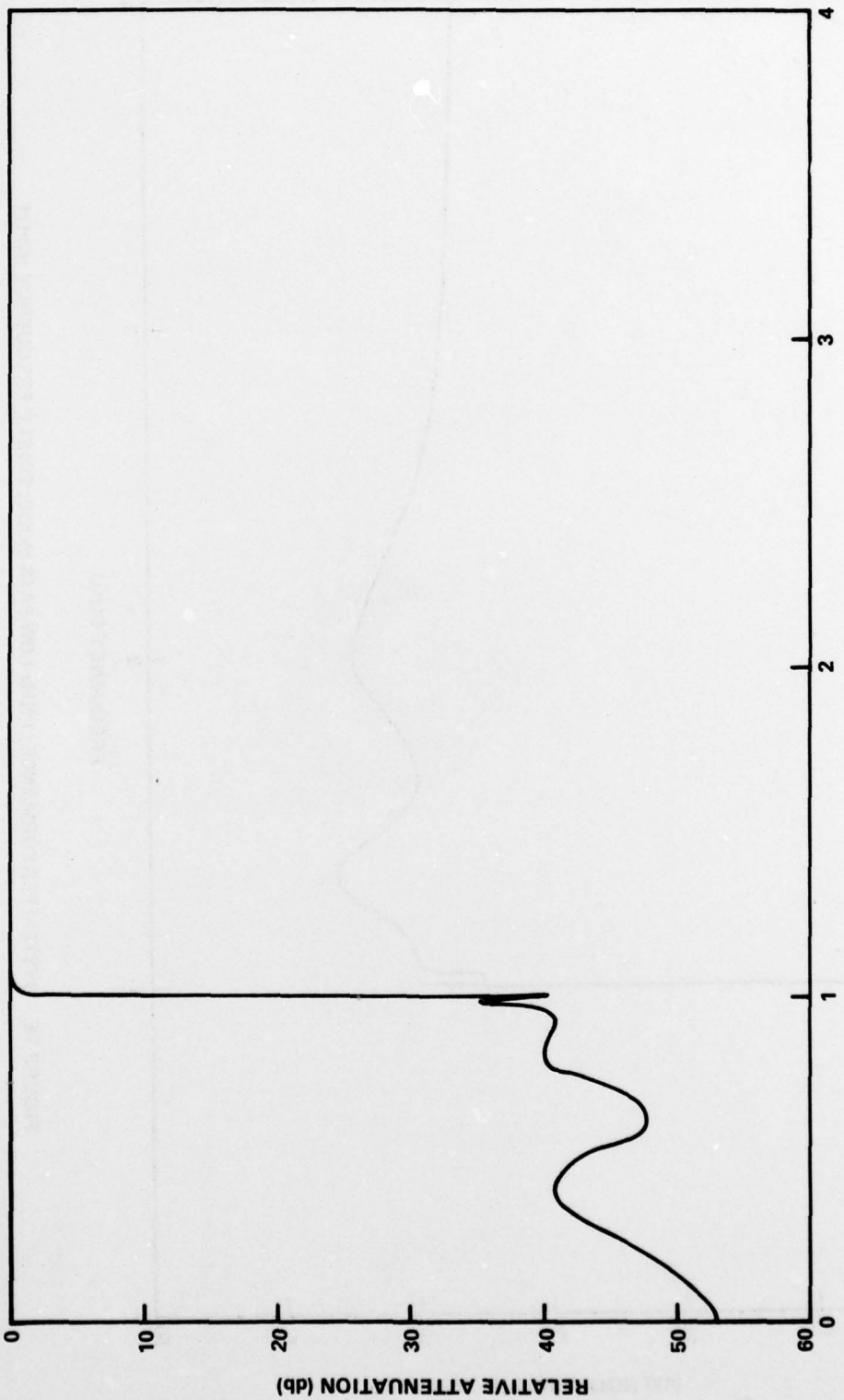


FIGURE 14. SYSTEM PERFORMANCE; 1 KHz HIGH-PASS MODE; SINGLE FREQUENCY INPUT

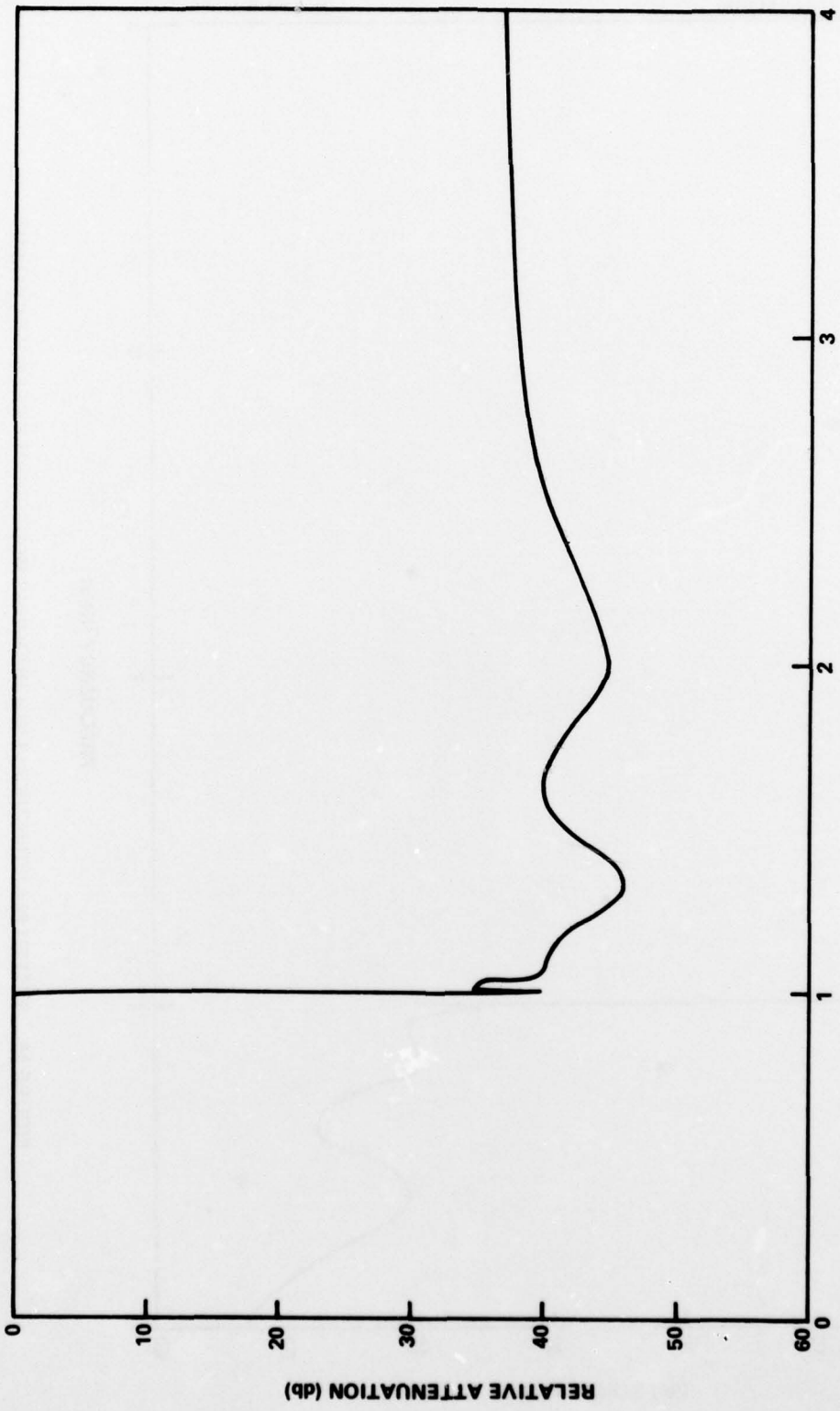


FIGURE 15. SYSTEM PERFORMANCE; 1 KHz LOW-PASS MODE; SINGLE FREQUENCY INPUT

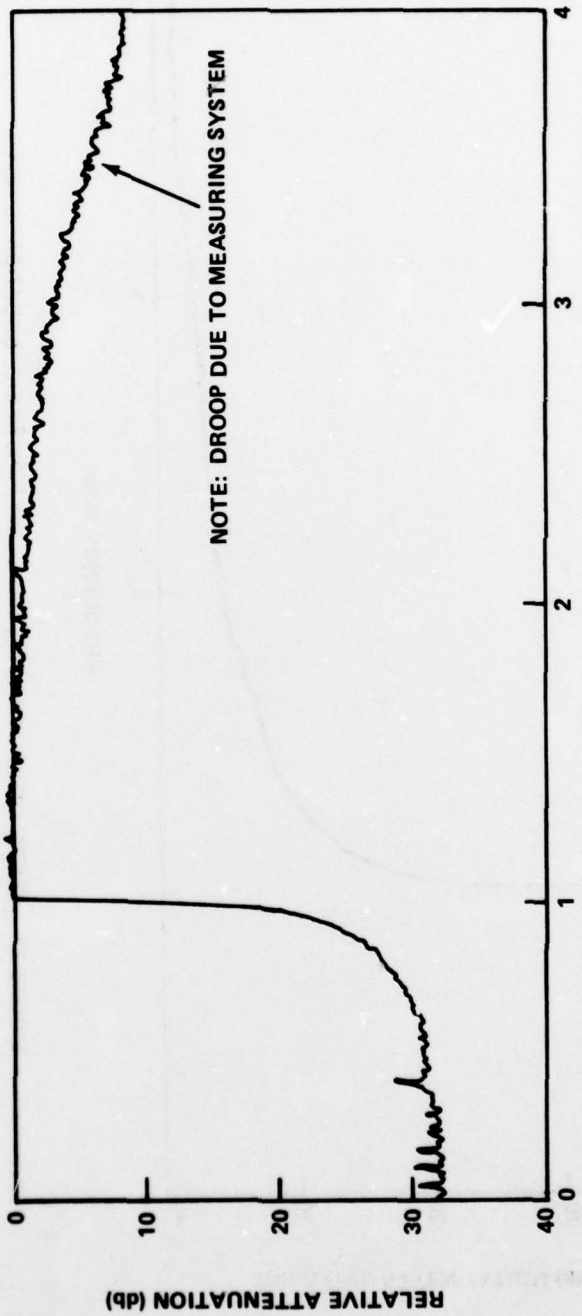


FIGURE 16. SYSTEM PERFORMANCE; 1 KHz HIGH-PASS MODE; BROADBAND INPUT

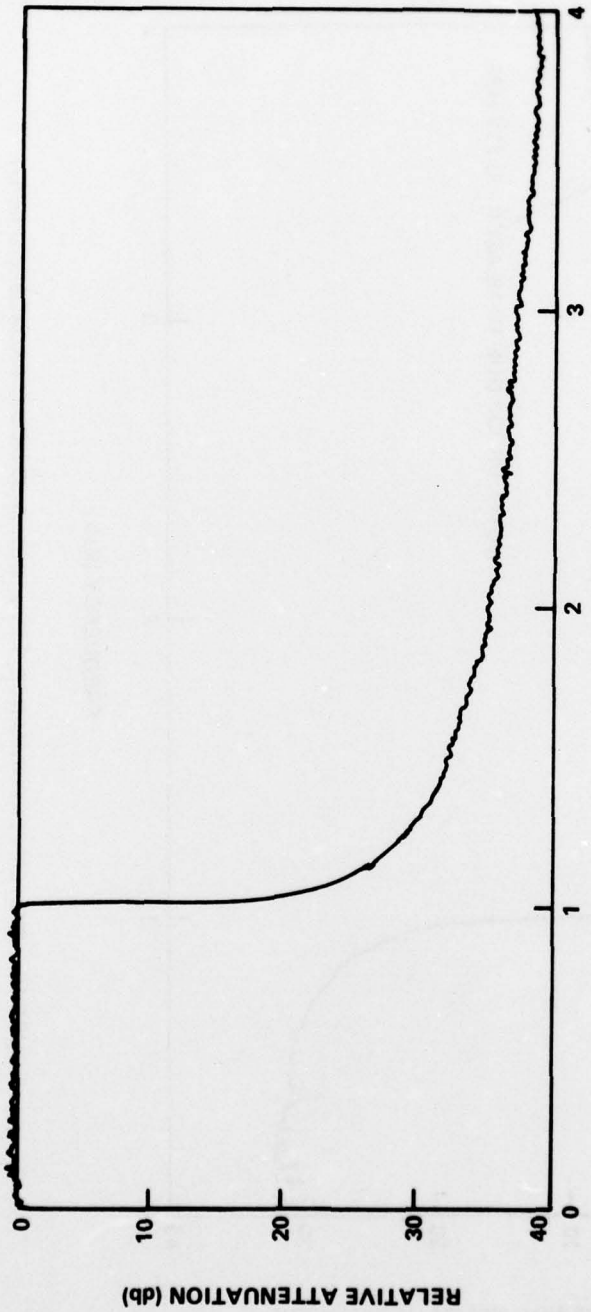


FIGURE 17. SYSTEM PERFORMANCE; 1 KHz LOW-PASS MODE; BROADBAND INPUT

APPENDIX A

PHASE-LOCK LOOP PARAMETERS

The natural frequency and damping ratio of a PLL are given respectively by reference (5).

$$\omega_N = \left(\frac{K_o K_D}{\tau_1}\right)^{\frac{1}{2}}$$

$$\delta = \frac{\tau_2}{2} \omega_N$$

where K_o is the VCO gain measured at the detector, K_D is the detector gain, τ_1 is the integrator time constant, and τ_2 is the time constant of the integrating capacitor and the direct path resistor (refer to Figure (12)).

The VCO characteristic is measured as 160 kHz/6.4 V = 157,000 rad/Vsec at the oscillator. This must divided by the divider setting, which is variable. Taking the mid-range setting, K_o = 157,000/105,000 = 1.5 rad/Vsec. The phase detector gain is K_D = 15V/2π rad = 2.4 V/rad. The integrator time constants are $\tau_1 = \tau_2$ = (1MΩ) (1μf) = 1 sec. The loop parameters are then:

$$\omega_N = \left(\frac{(1.5)\ (2.4)}{1}\right)^{\frac{1}{2}} = 1.8 \text{ rad/sec}$$

$$\delta = \frac{1}{2}\ (1.8) = 0.9$$

The addition of the capacitor across the direct path resistor is not included in the analysis; its effect is to reduce both quantities slightly.

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[5] F. M. Gardner, Wiley, "Phaselock Techniques," 1966.